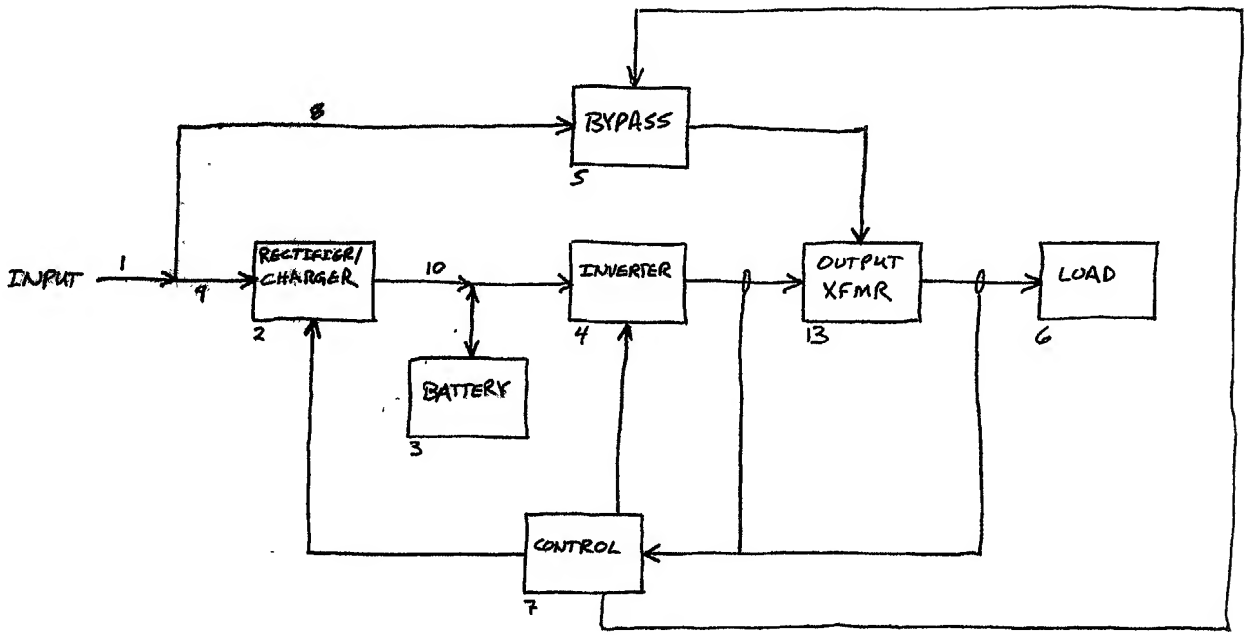


Fig. 1

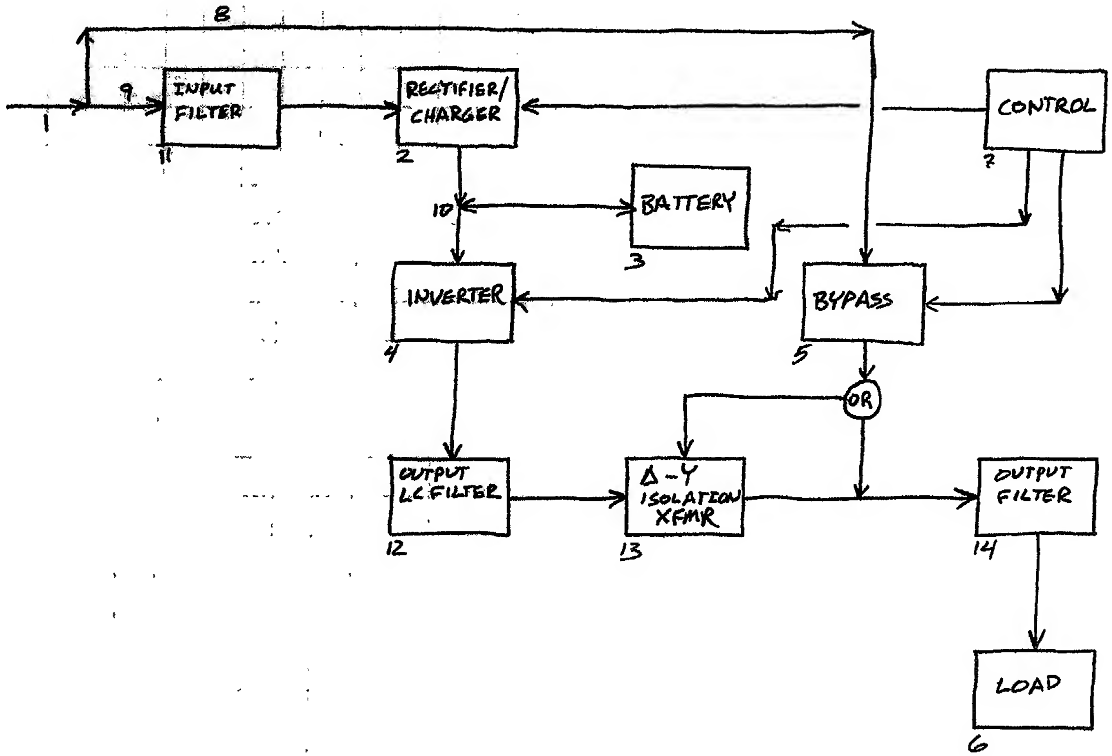

INPUT FILTER
RECTIFIER/ CHARGER
CONTROL
BATTERY
INVERTER
BYPASS
OR
OUTPUT LC FILTER
Δ-Y ISOLATION XFMR
OUTPUT FILTER
LOAD
1
2
3
4
5
6
7
8
9
10
11
12
13
14

Fig. 2

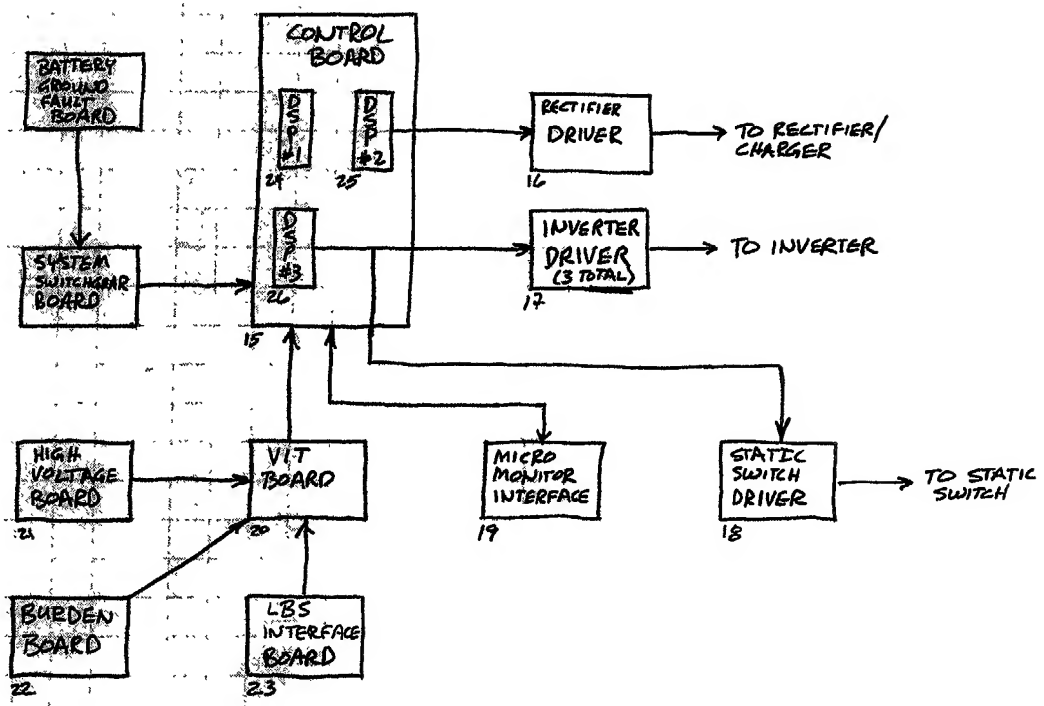

CONTROL BOARD
DSP #1
DSP #2
DSP #3
24
25
26
15
BATTERY GROUND FAULT BOARD
SYSTEM SWITCHGEAR BOARD
RECTIFIER DRIVER
16
TO RECTIFIER/ CHARGER
INVERTER DRIVER (3 TOTAL)
17
TO INVERTER
HIGH VOLTAGE BOARD
21
VIT BOARD
20
MICRO MONITOR INTERFACE
19
STATIC SWITCH DRIVER
18
TO STATIC SWITCH
BURDEN BOARD
22
LBS INTERFACE BOARD
23

Fig. 3

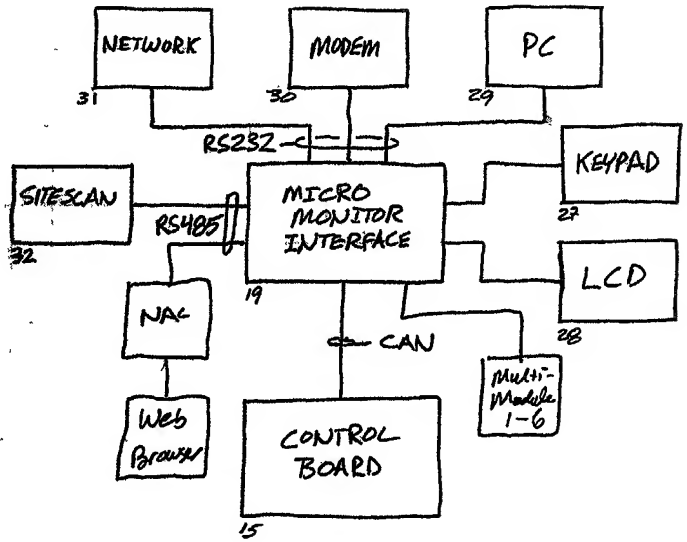

NETWORK
MODEM
PC
31
30
29
RS232
KEYPAD
SITESCAN
MICRO
MONITOR
INTERFACE
RS485
27
32
19
LCD
NAC
CAN
28
Multi-
Module
1-6
Web
Browser
CONTROL
BOARD
15

Fig. 4

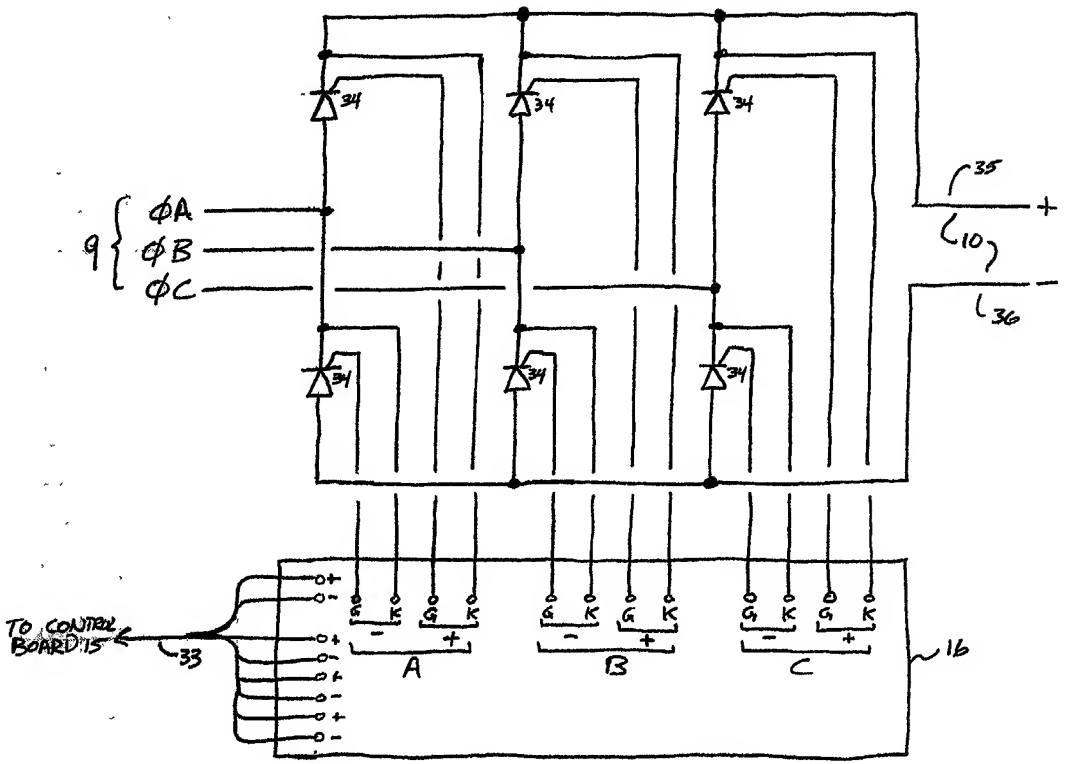

34
34
34
34
34
34
35
+
10
36
−
9
ΦA
ΦB
ΦC
TO CONTROL BOARD 15
33
G
K
A
B
C
16

Fig. 5

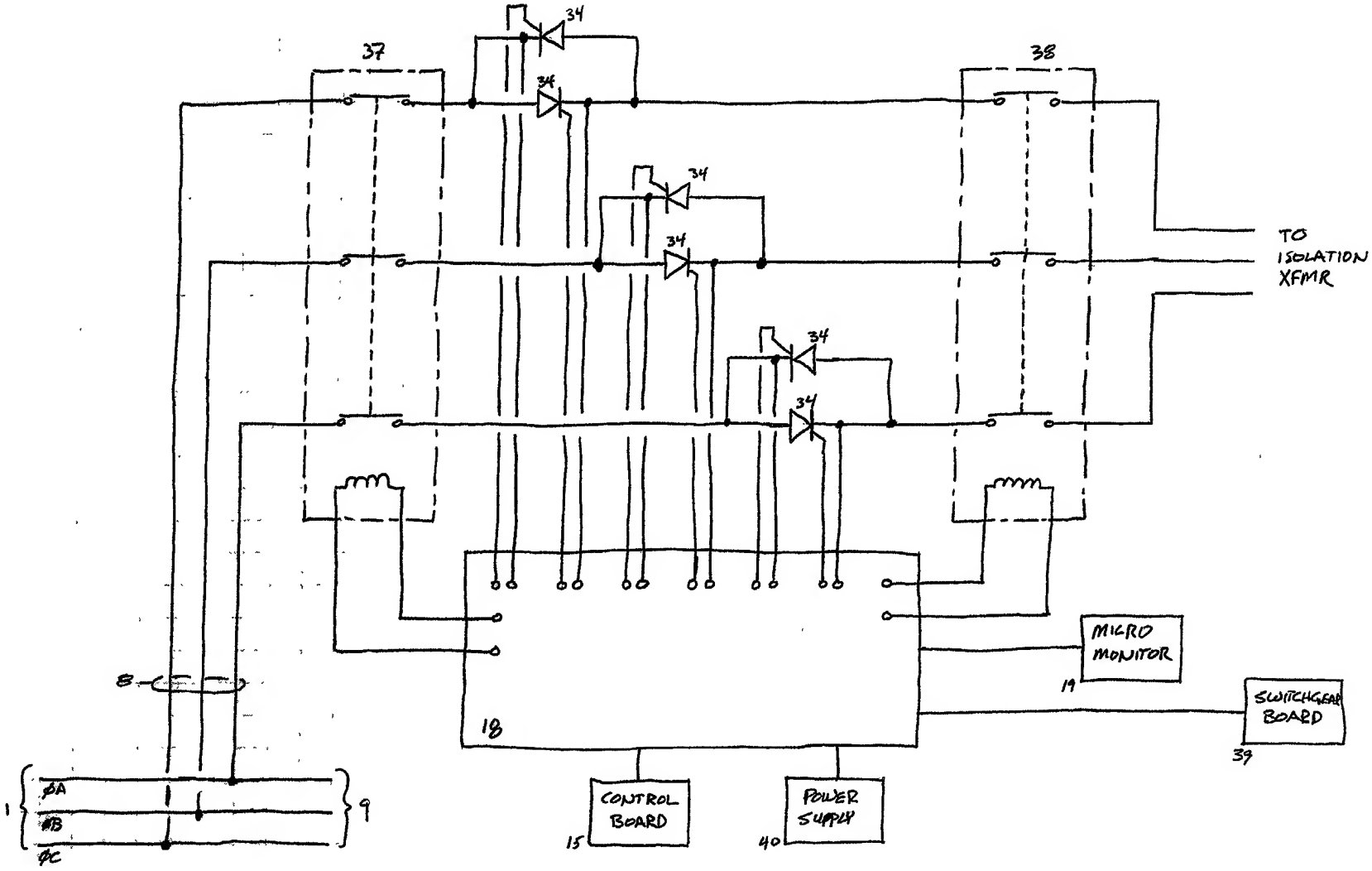


Fig. 6

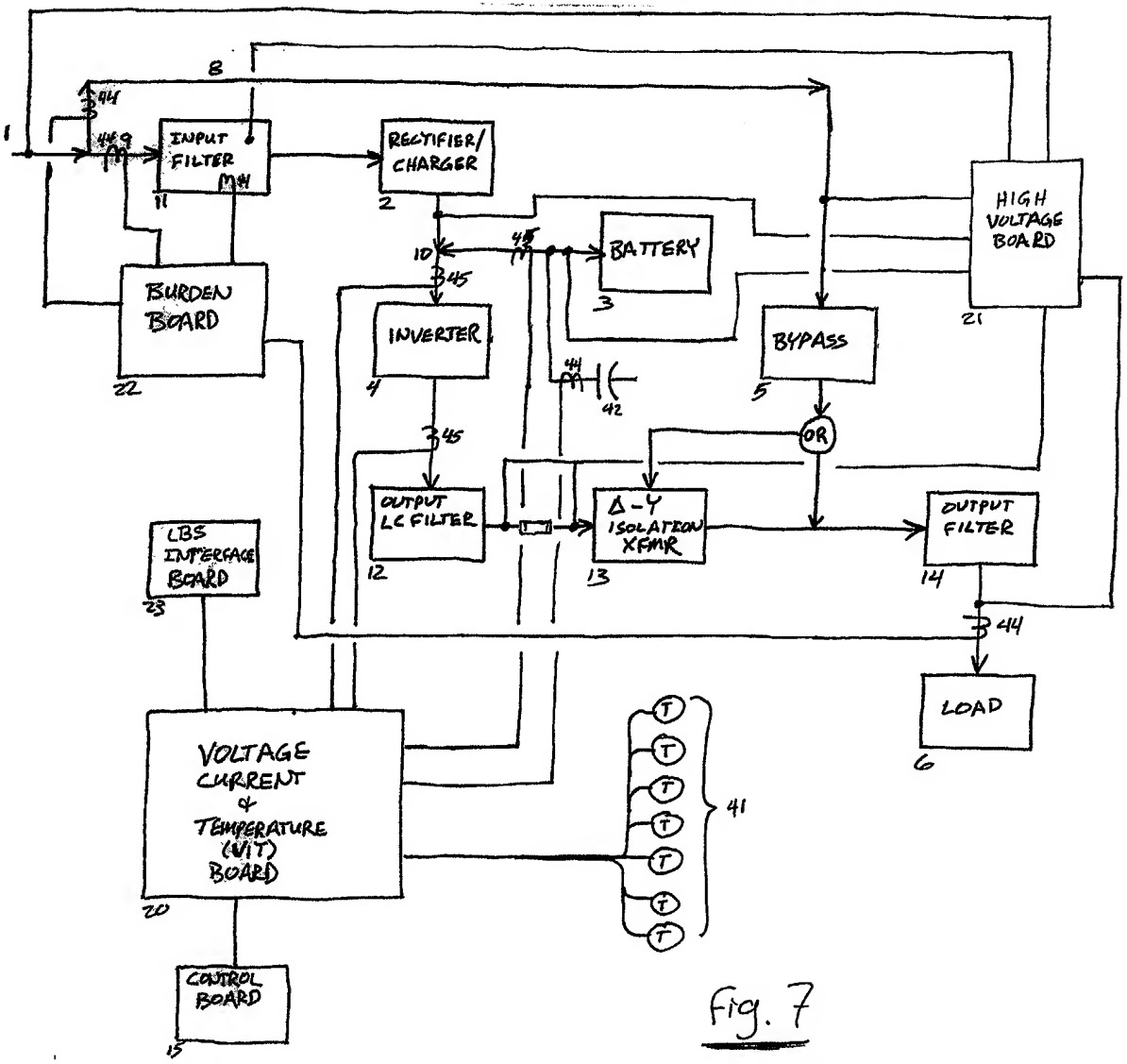

8
1
44
49
INPUT FILTER
11
RECTIFIER/ CHARGER
2
HIGH VOLTAGE BOARD
21
10
45
BATTERY
3
BURDEN BOARD
22
INVERTER
4
BYPASS
5
42
OR
45
OUTPUT LC FILTER
12
Δ-Y ISOLATION XFMR
13
OUTPUT FILTER
14
LBS INTERFACE BOARD
23
44
LOAD
6
VOLTAGE CURRENT & TEMPERATURE (V/I/T) BOARD
20
T
41
CONTROL BOARD
15

Fig. 7

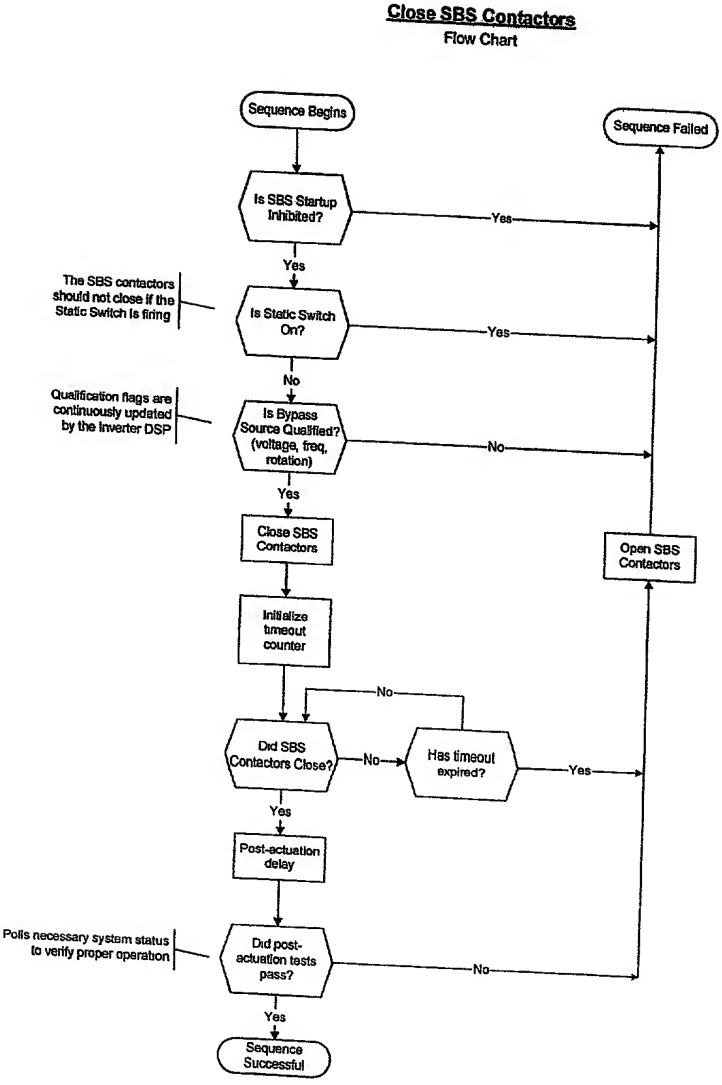

Close SBS Contactors
Flow Chart
Sequence Begins
Sequence Failed
Is SBS Startup Inhibited?
Yes
Yes
The SBS contactors should not close if the Static Switch is firing
Is Static Switch On?
Yes
No
Qualification flags are continuously updated by the inverter DSP
Is Bypass Source Qualified? (voltage, freq, rotation)
No
Yes
Close SBS Contactors
Open SBS Contactors
Initialize timeout counter
No
Did SBS Contactors Close?
No
Has timeout expired?
Yes
Yes
Post-actuation delay
Polls necessary system status to verify proper operation
Did post-actuation tests pass?
No
Yes
Sequence Successful

Fig. 8

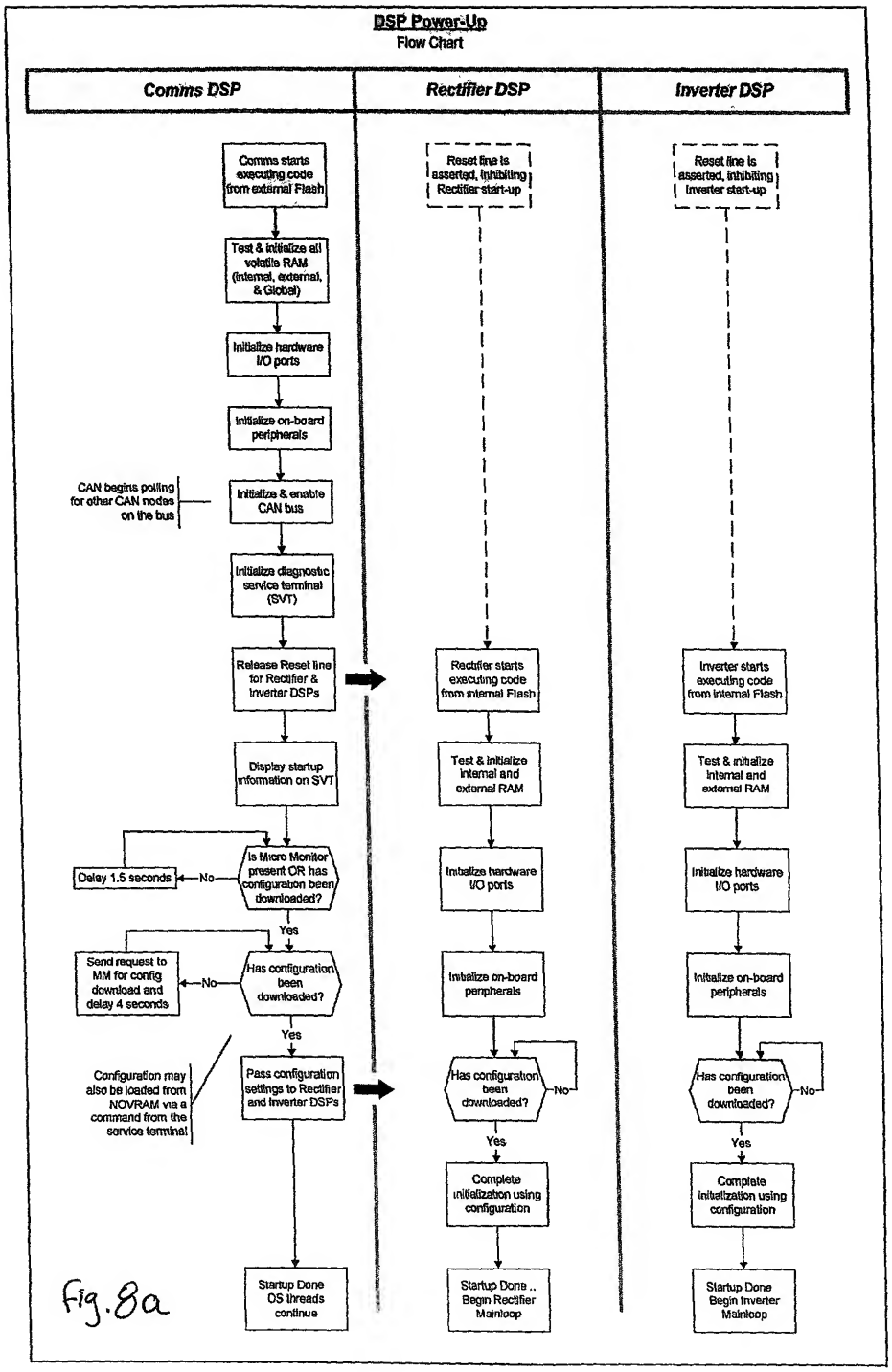

DSP Power-Up
Flow Chart
Comms DSP
Rectifier DSP
Inverter DSP
Comms starts executing code from external Flash
Reset line is asserted, inhibiting Rectifier start-up
Reset line is asserted, inhibiting Inverter start-up
Test & initialize all volatile RAM (internal, external, & Global)
Initialize hardware I/O ports
Initialize on-board peripherals
CAN begins polling for other CAN nodes on the bus
Initialize & enable CAN bus
Initialize diagnostic service terminal (SVT)
Release Reset line for Rectifier & Inverter DSPs
Rectifier starts executing code from internal Flash
Inverter starts executing code from internal Flash
Display startup information on SVT
Test & initialize internal and external RAM
Test & initialize internal and external RAM
Delay 1.5 seconds
No
Is Micro Monitor present OR has configuration been downloaded?
Initialize hardware I/O ports
Initialize hardware I/O ports
Yes
Send request to MM for config download and delay 4 seconds
No
Has configuration been downloaded?
Initialize on-board peripherals
Initialize on-board peripherals
Yes
Configuration may also be loaded from NOVRAM via a command from the service terminal
Pass configuration settings to Rectifier and Inverter DSPs
Has configuration been downloaded?
No
Has configuration been downloaded?
No
Yes
Complete initialization using configuration
Complete initialization using configuration
Yes
Startup Done OS threads continue
Startup Done .. Begin Rectifier Mainloop
Startup Done Begin Inverter Mainloop

Fig. 8a

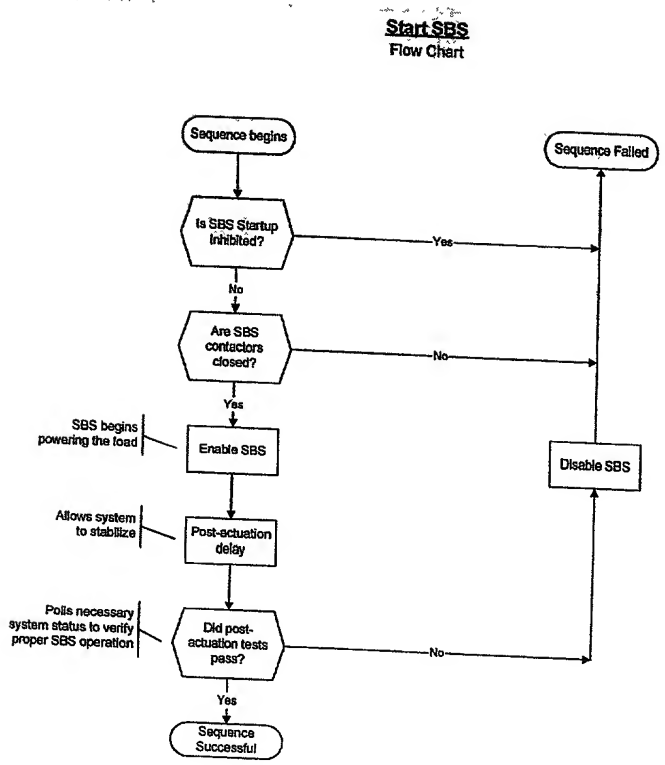

Start SBS
Flow Chart
Sequence begins
Sequence Failed
Is SBS Startup Inhibited?
Yes
No
Are SBS contactors closed?
No
Yes
SBS begins powering the load
Enable SBS
Disable SBS
Allows system to stabilize
Post-actuation delay
Polls necessary system status to verify proper SBS operation
Did post-actuation tests pass?
No
Yes
Sequence Successful

Fig. 9

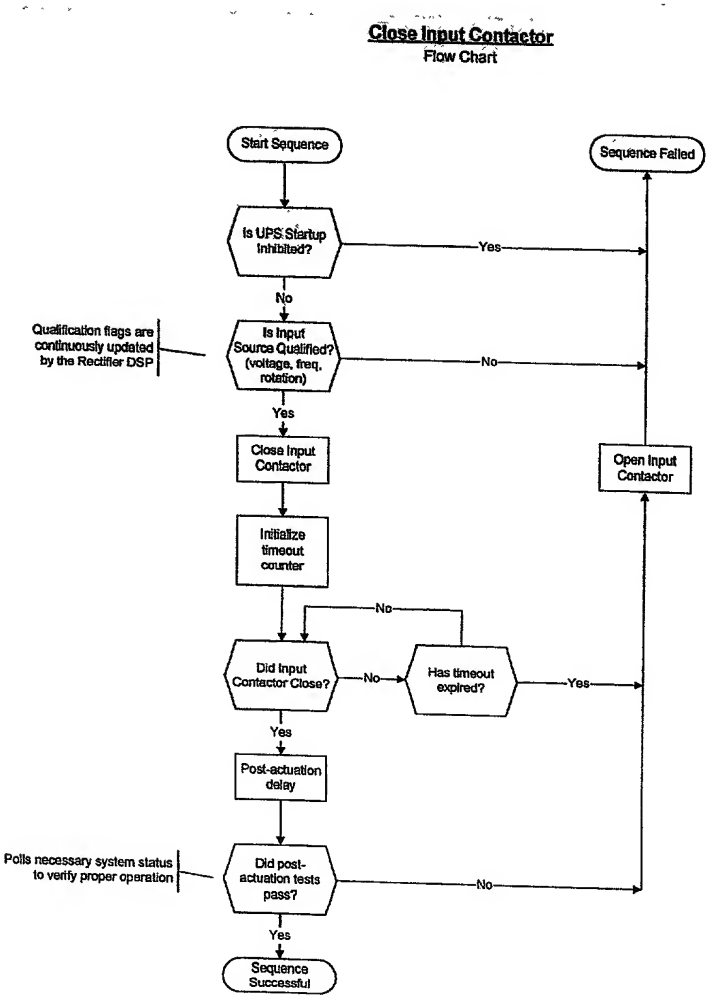

Close Input Contactor
Flow Chart
Start Sequence
Sequence Failed
Is UPS Startup Inhibited?
Yes
No
Qualification flags are continuously updated by the Rectifier DSP
Is Input Source Qualified? (voltage, freq, rotation)
No
Yes
Close Input Contactor
Open Input Contactor
Initialize timeout counter
No
Did Input Contactor Close?
No
Has timeout expired?
Yes
Yes
Post-actuation delay
Polls necessary system status to verify proper operation
Did post-actuation tests pass?
No
Yes
Sequence Successful

Fig. 10

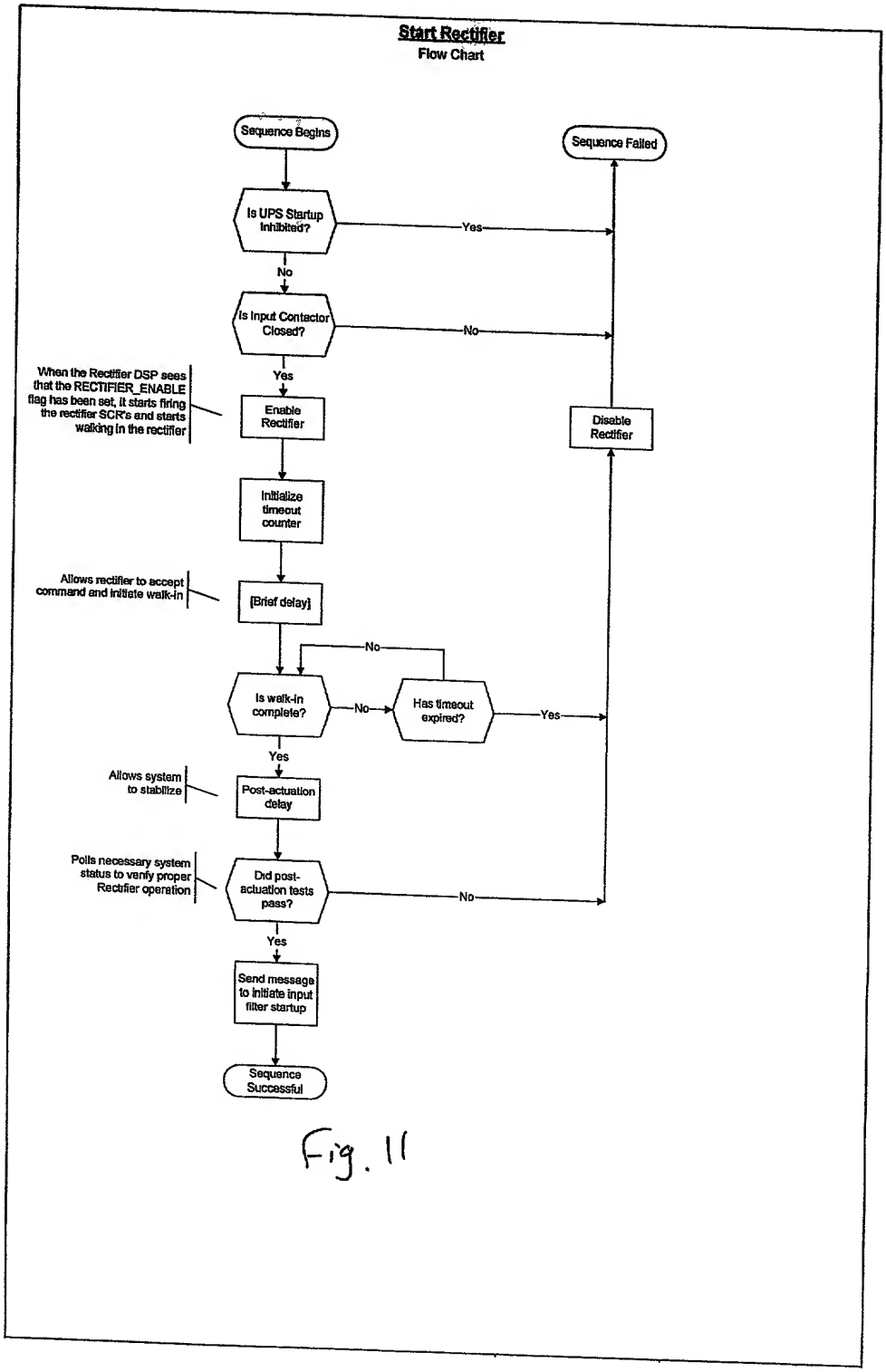

Start Rectifier
Flow Chart
Sequence Begins
Sequence Failed
Is UPS Startup Inhibited?
Yes
No
Is Input Contactor Closed?
No
Yes
When the Rectifier DSP sees that the RECTIFIER_ENABLE flag has been set, it starts firing the rectifier SCR's and starts walking in the rectifier
Enable Rectifier
Disable Rectifier
Initialize timeout counter
Allows rectifier to accept command and initiate walk-in
[Brief delay]
No
Is walk-in complete?
No
Has timeout expired?
Yes
Yes
Allows system to stabilize
Post-actuation delay
Polls necessary system status to verify proper Rectifier operation
Did post-actuation tests pass?
No
Yes
Send message to initiate input filter startup
Sequence Successful

Fig. 11

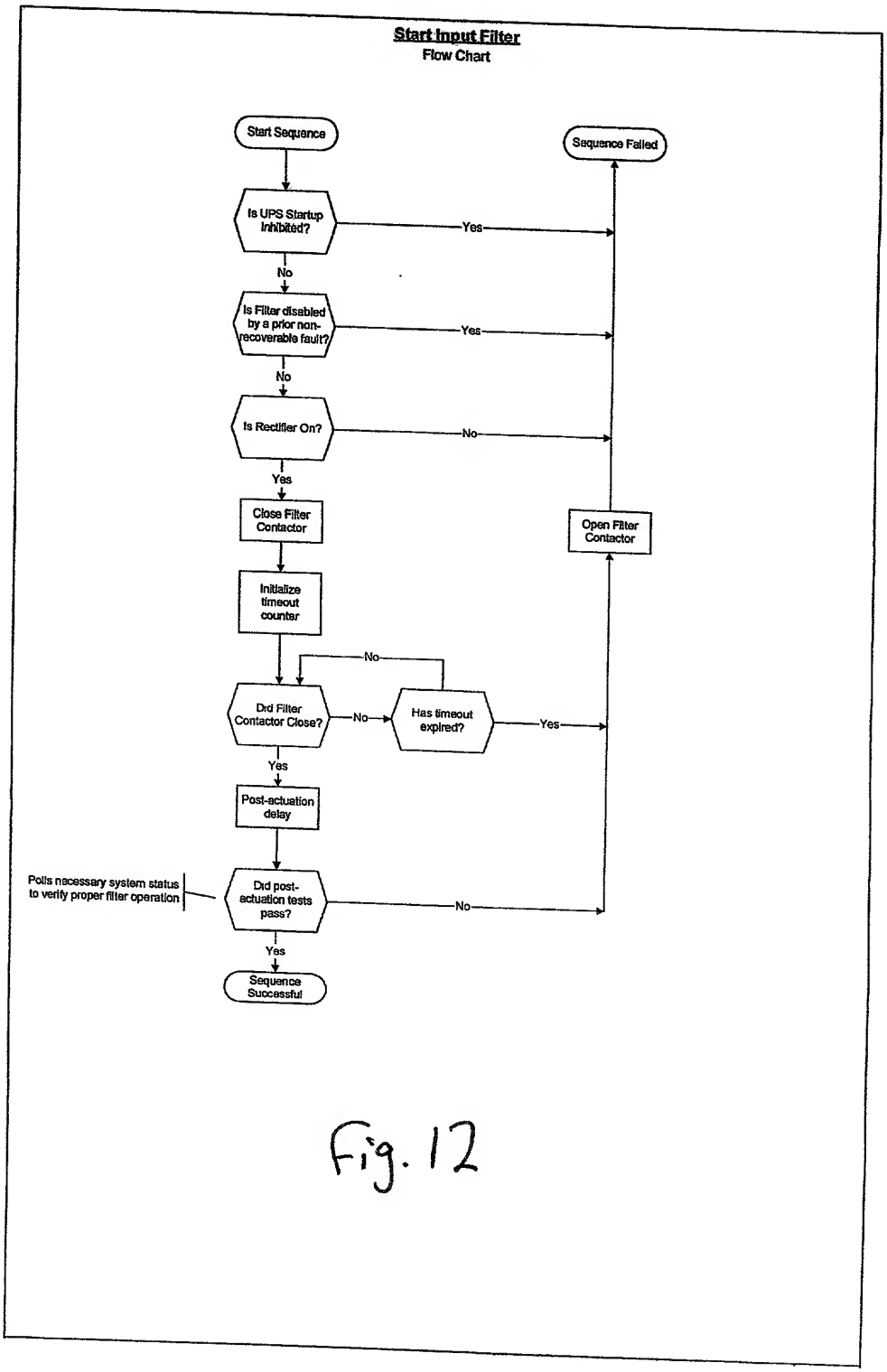

Start Input Filter
Flow Chart
Start Sequence
Sequence Failed
Is UPS Startup Inhibited?
Yes
No
Is Filter disabled by a prior non-recoverable fault?
Yes
No
Is Rectifier On?
No
Yes
Close Filter Contactor
Open Filter Contactor
Initialize timeout counter
No
Did Filter Contactor Close?
No
Has timeout expired?
Yes
Yes
Post-actuation delay
Polls necessary system status to verify proper filter operation
Did post-actuation tests pass?
No
Yes
Sequence Successful

Fig. 12

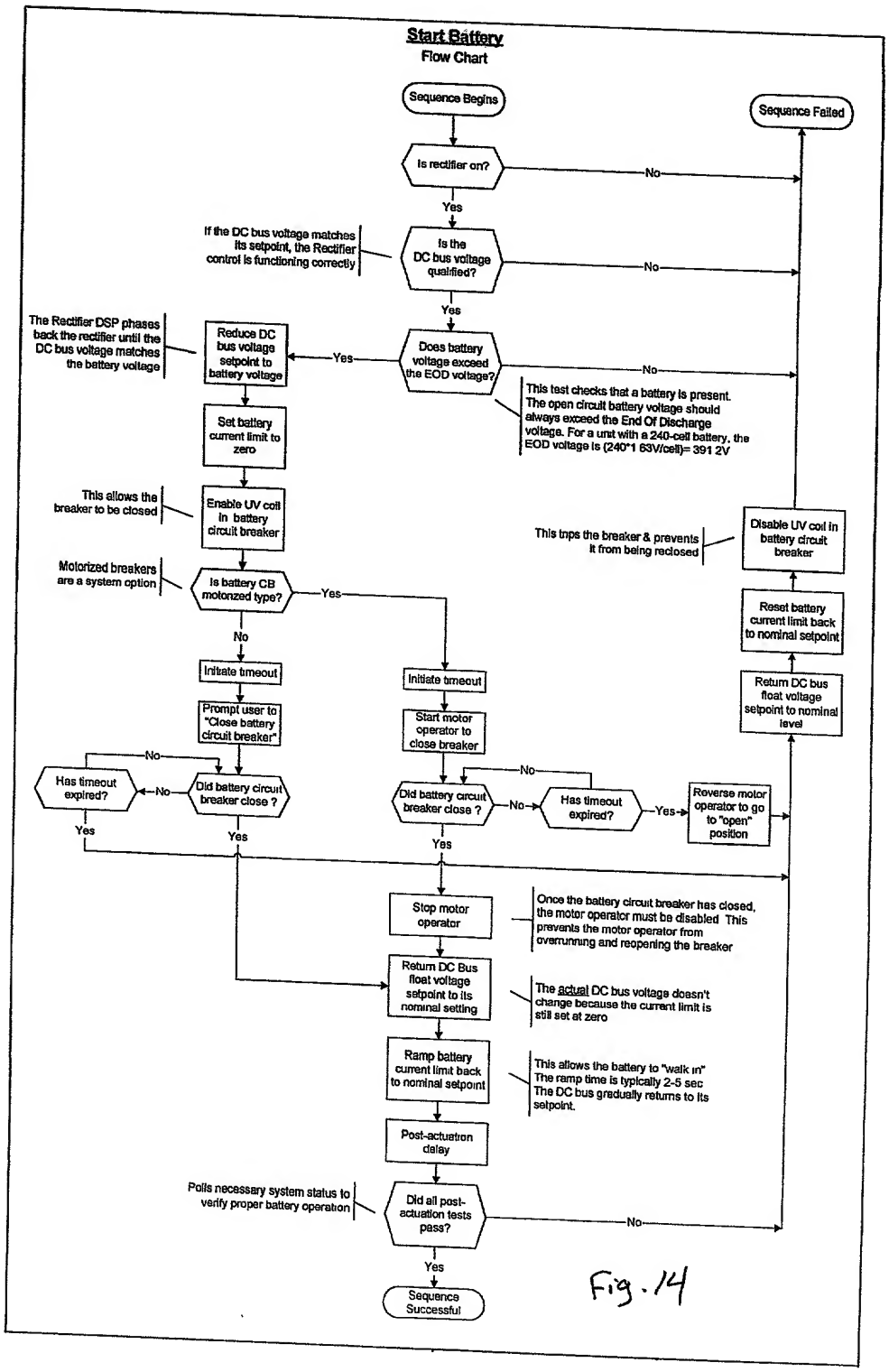

Start Battery
Flow Chart
Sequence Begins
Sequence Failed
Is rectifier on?
No
Yes
If the DC bus voltage matches its setpoint, the Rectifier control is functioning correctly
Is the DC bus voltage qualified?
No
Yes
The Rectifier DSP phases back the rectifier until the DC bus voltage matches the battery voltage
Reduce DC bus voltage setpoint to battery voltage
Yes
Does battery voltage exceed the EOD voltage?
No
This test checks that a battery is present. The open circuit battery voltage should always exceed the End Of Discharge voltage. For a unit with a 240-cell battery, the EOD voltage is (240*1 63V/cell)= 391 2V
Set battery current limit to zero
This allows the breaker to be closed
Enable UV coil in battery circuit breaker
This trips the breaker & prevents it from being reclosed
Disable UV coil in battery circuit breaker
Motorized breakers are a system option
Is battery CB motorized type?
Yes
No
Initiate timeout
Prompt user to "Close battery circuit breaker"
Has timeout expired?
No
Yes
Did battery circuit breaker close ?
No
Yes
Initiate timeout
Start motor operator to close breaker
Did battery circuit breaker close ?
No
Yes
Has timeout expired?
Yes
Reverse motor operator to go to "open" position
Reset battery current limit back to nominal setpoint
Return DC bus float voltage setpoint to nominal level
Stop motor operator
Once the battery circuit breaker has closed, the motor operator must be disabled This prevents the motor operator from overrunning and reopening the breaker
Return DC Bus float voltage setpoint to its nominal setting
The actual DC bus voltage doesn't change because the current limit is still set at zero
Ramp battery current limit back to nominal setpoint
This allows the battery to "walk in" The ramp time is typically 2-5 sec The DC bus gradually returns to its setpoint.
Post-actuation delay
Polls necessary system status to verify proper battery operation
Did all post-actuation tests pass?
No
Yes
Sequence Successful

Fig. 14

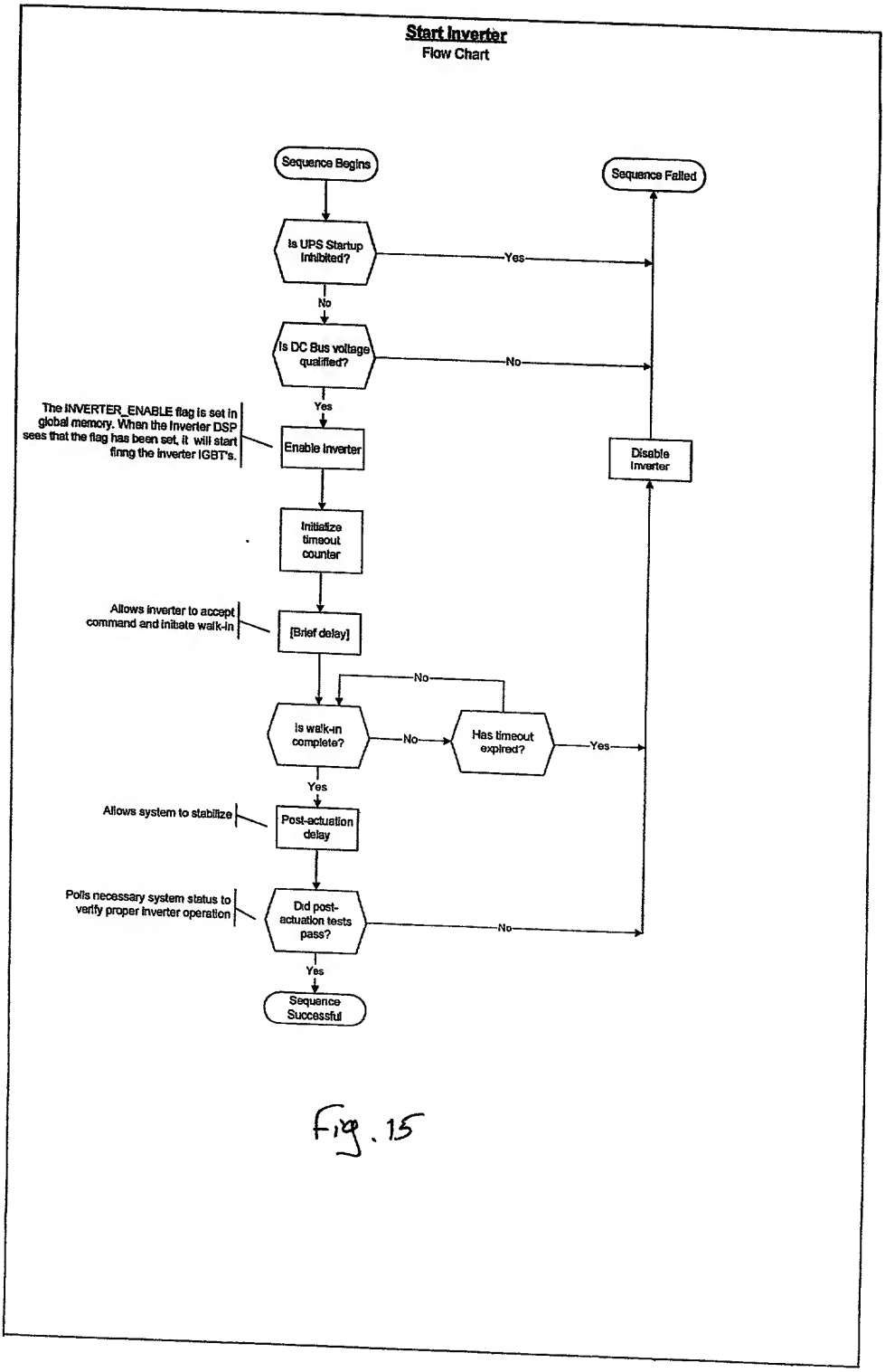

Start Inverter
Flow Chart
Sequence Begins
Sequence Failed
Is UPS Startup Inhibited?
Yes
No
Is DC Bus voltage qualified?
No
Yes
The INVERTER_ENABLE flag is set in global memory. When the Inverter DSP sees that the flag has been set, it will start firing the inverter IGBT's.
Enable Inverter
Disable Inverter
Initialize timeout counter
Allows inverter to accept command and initiate walk-in
[Brief delay]
No
Is walk-in complete?
No
Has timeout expired?
Yes
Yes
Allows system to stabilize
Post-actuation delay
Polls necessary system status to verify proper inverter operation
Did post-actuation tests pass?
No
Yes
Sequence Successful

Fig. 15

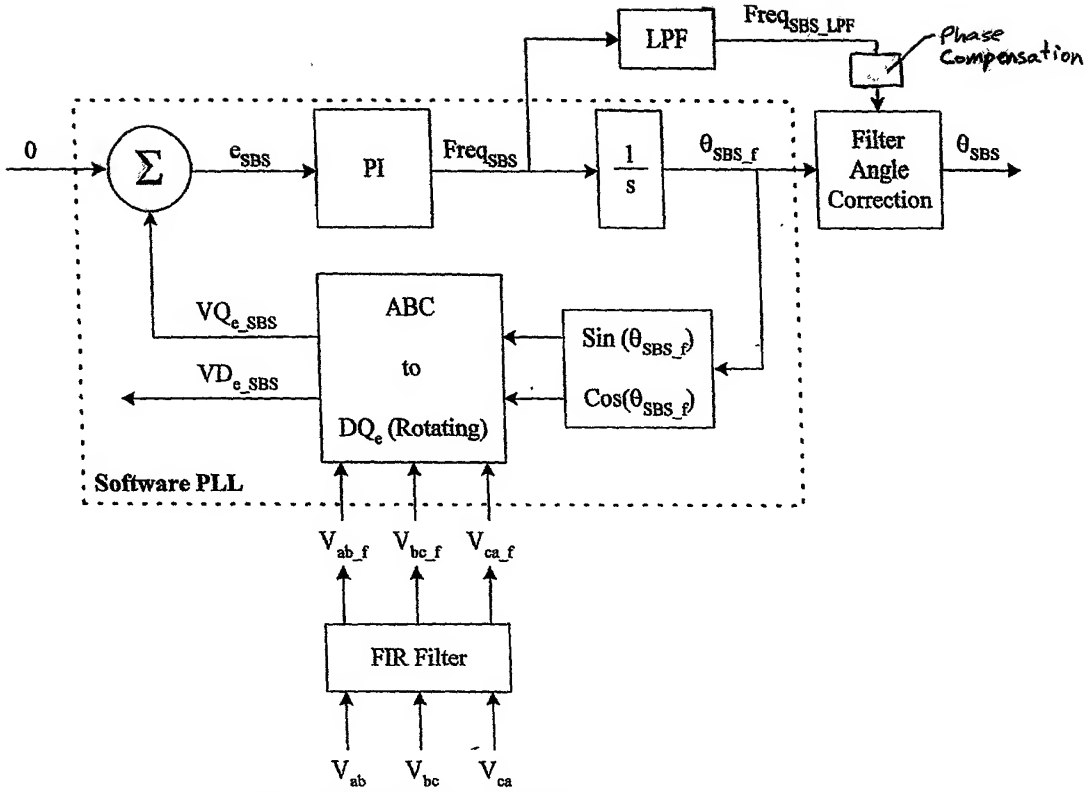

LPF
$Freq_{SBS\_LPF}$
Phase Compensation
0
Σ
e_{SBS}
PI
$Freq_{SBS}$
1/s
θ_{SBS_f}
Filter Angle Correction
θ_{SBS}
VQ_{e_SBS}
VD_{e_SBS}
ABC to DQ_e (Rotating)
Sin (θ_{SBS_f})
Cos(θ_{SBS_f})
Software PLL
V_{ab_f} V_{bc_f} V_{ca_f}
FIR Filter
V_{ab} V_{bc} V_{ca}
Static Bypass Switch L-L Voltages

Fig. 16

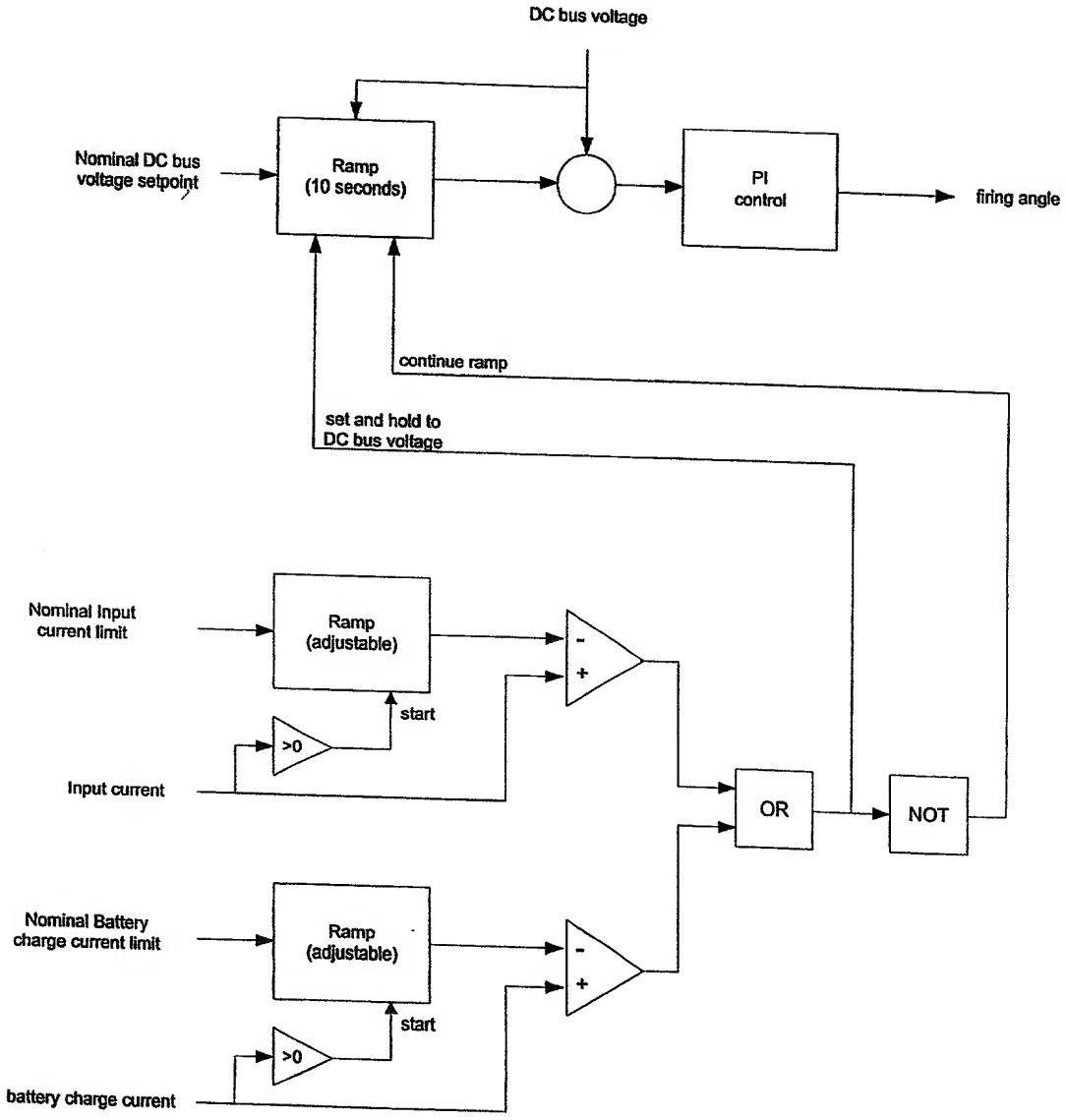

DC bus voltage
Nominal DC bus voltage setpoint
Ramp (10 seconds)
PI control
firing angle
continue ramp
set and hold to DC bus voltage
Nominal Input current limit
Ramp (adjustable)
start
>0
Input current
OR
NOT
Nominal Battery charge current limit
Ramp (adjustable)
start
>0
battery charge current

Fig. 17a

Rectifier Control Block Diagram

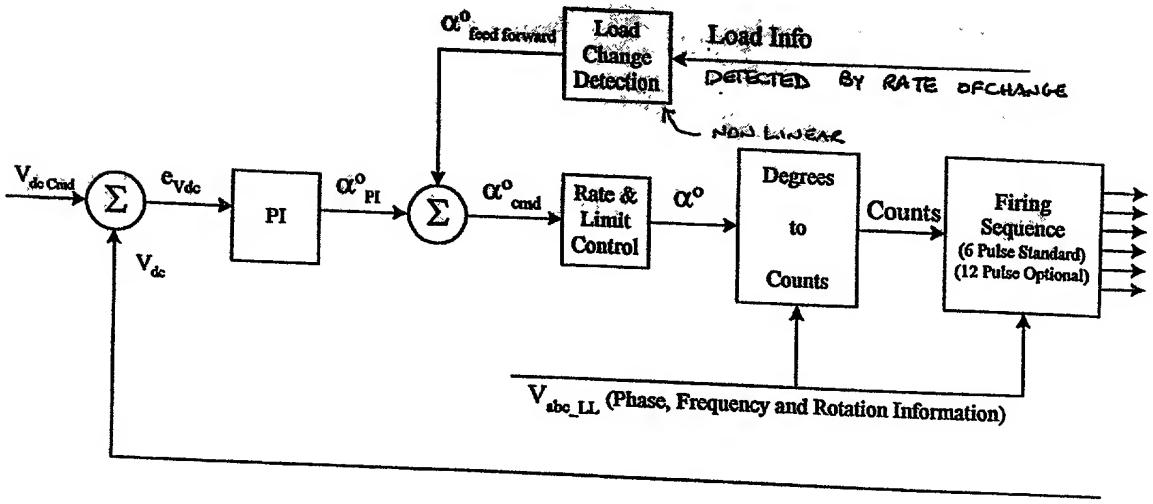


Fig. 17b

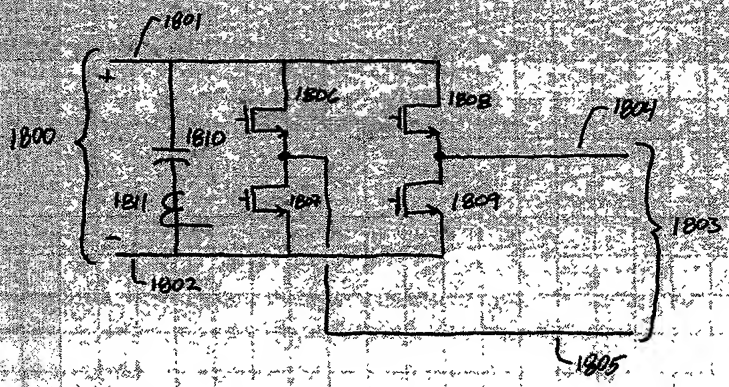


Fig. 18A

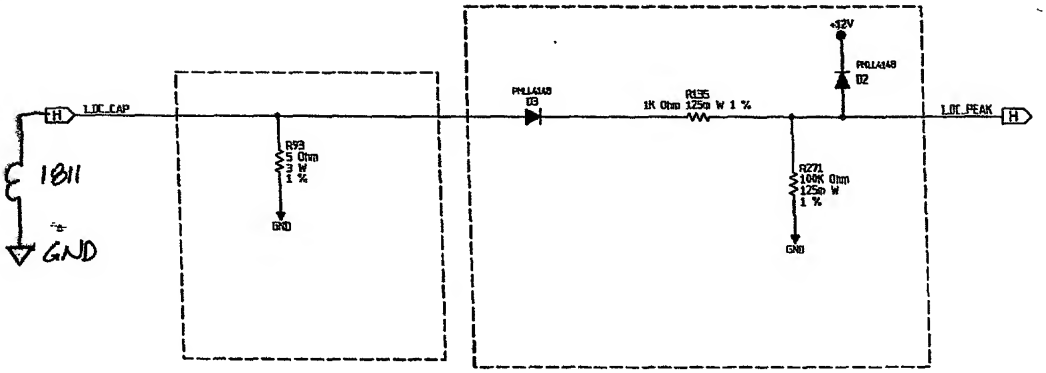


Fig. 18B

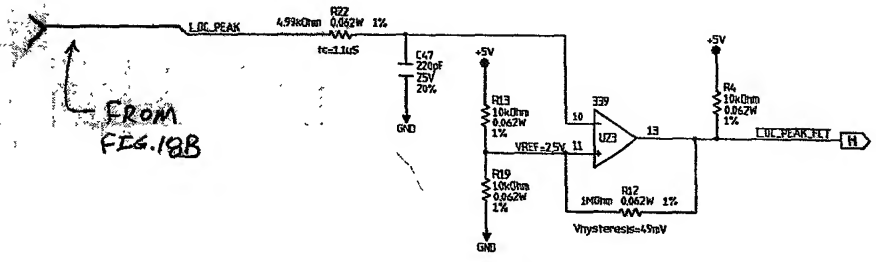


Fig. 18C

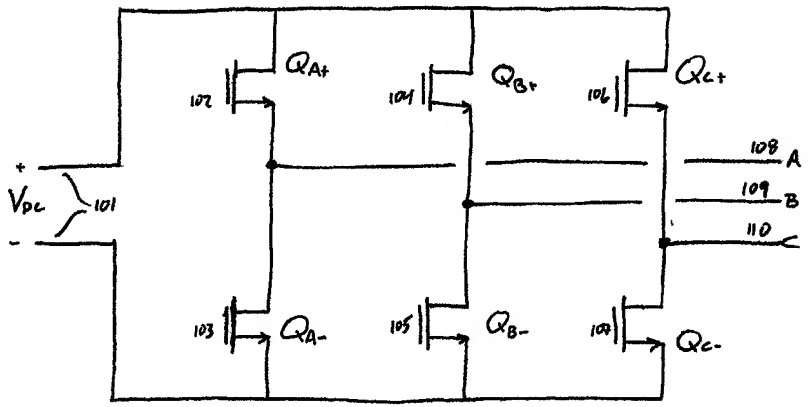
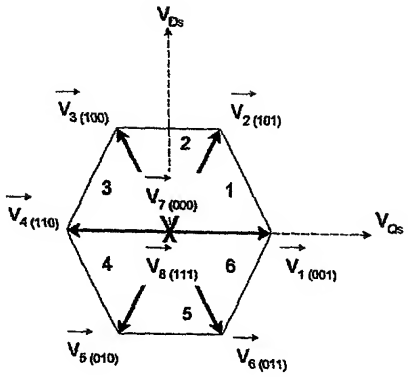


Fig. 19

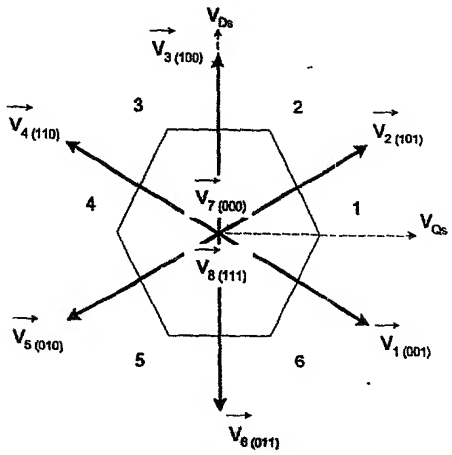
Switch (0 = OFF, 1 = ON)			Line to Neutral Voltage Vectors					Line to Line Voltage Vectors				
S_{C+}	S_{B+}	S_{A+}	V_{AN}	V_{BN}	V_{CN}	$V = [V_{Qs}\ V_{Ds}]^T$	Vector	V_{AB}	V_{BC}	V_{CA}	$V = [V_{Qs}\ V_{Ds}]^T$	Vector
0	0	1	$2/3\ V_{dc}$	$-1/3\ V_{dc}$	$-1/3\ V_{dc}$	$2/3\ V_{dc}\ \angle 0°$	$\vec{V}_1$	V_{dc}	0	$-V_{dc}$	$2/\sqrt{3}\ V_{dc}\ \angle -30°$	$\vec{V}_1$
1	0	1	$1/3\ V_{dc}$	$-2/3\ V_{dc}$	$1/3\ V_{dc}$	$2/3\ V_{dc}\ \angle 60°$	$\vec{V}_2$	V_{dc}	$-V_{dc}$	0	$2/\sqrt{3}\ V_{dc}\ \angle 30°$	$\vec{V}_2$
1	0	0	$-1/3\ V_{dc}$	$-1/3\ V_{dc}$	$2/3\ V_{dc}$	$2/3\ V_{dc}\ \angle 120°$	$\vec{V}_3$	0	$-V_{dc}$	V_{dc}	$2/\sqrt{3}\ V_{dc}\ \angle 90°$	$\vec{V}_3$
1	1	0	$-2/3\ V_{dc}$	$1/3\ V_{dc}$	$1/3\ V_{dc}$	$2/3\ V_{dc}\ \angle 180°$	$\vec{V}_4$	$-V_{dc}$	0	V_{dc}	$2/\sqrt{3}\ V_{dc}\ \angle 150°$	$\vec{V}_4$
0	1	0	$-1/3\ V_{dc}$	$2/3\ V_{dc}$	$-1/3\ V_{dc}$	$2/3\ V_{dc}\ \angle 240°$	$\vec{V}_5$	$-V_{dc}$	V_{dc}	0	$2/\sqrt{3}\ V_{dc}\ \angle 210°$	$\vec{V}_5$
0	1	1	$1/3\ V_{dc}$	$1/3\ V_{dc}$	$-2/3\ V_{dc}$	$2/3\ V_{dc}\ \angle 300°$	$\vec{V}_6$	0	V_{dc}	$-V_{dc}$	$2/\sqrt{3}\ V_{dc}\ \angle 270°$	$\vec{V}_6$
0	0	0	0	0	0	0	$\vec{V}_7$	0	0	0	0	$\vec{V}_7$
1	1	1	0	0	0	0	$\vec{V}_8$	0	0	0	0	$\vec{V}_8$

Possible Switch Combinations (note: 0 = Switch OFF, 1 = Switch ON), Equivalent Line to Neutral Voltage Vectors and Equivalent Line to Line Voltage Vectors.

Fig. 20



Line to Neutral Voltage Vectors Projected Onto The DQs Axis (Note: (001) = S_C, OFF, S_B, OFF, S_A, ON)



Line to Line Voltage Vectors Projected Onto The DQs Axis (Note: (001) = S_C, OFF, S_B, OFF, S_A, ON)

Fig. 21

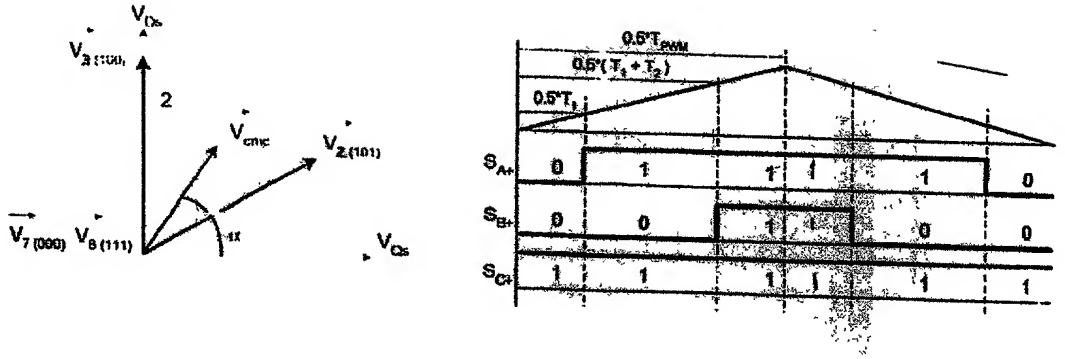


Fig. 22

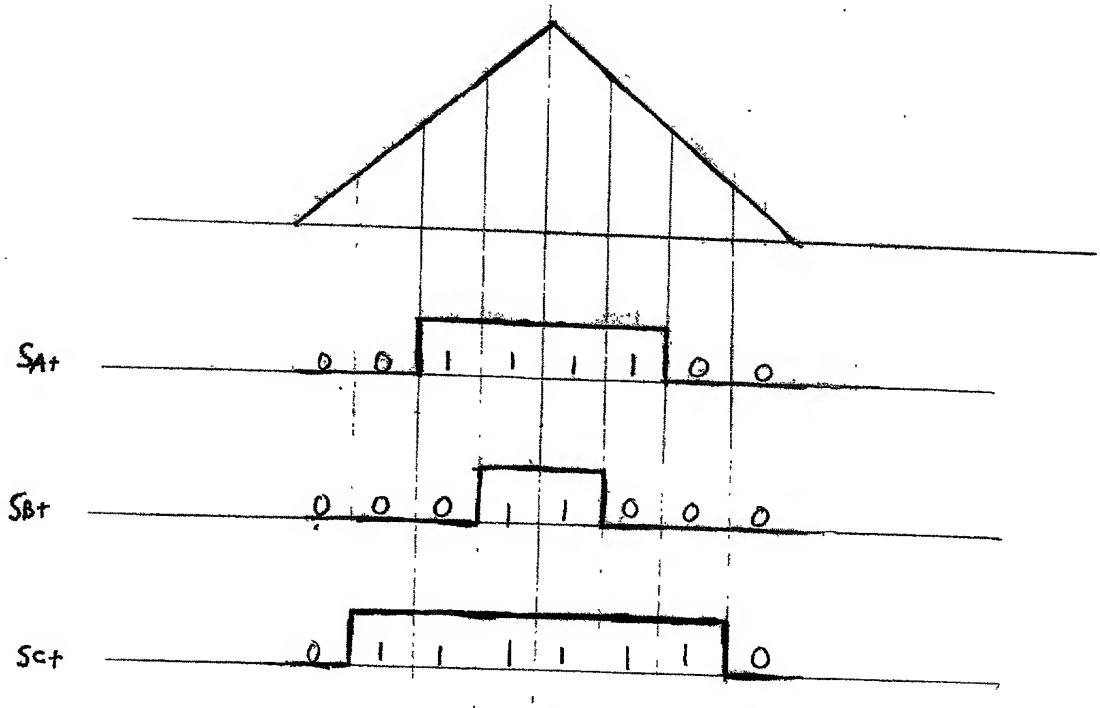


Fig. 22a

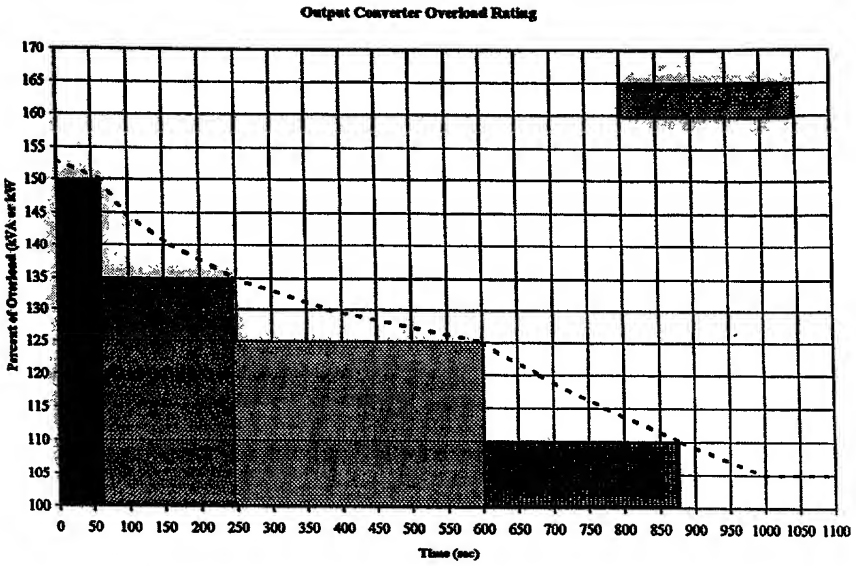

Output Converter Overload Rating
Percent of Overload (kVA or kW
170
165
160
155
150
145
140
135
130
125
120
115
110
105
100
0 50 100 150 200 250 300 350 400 450 500 550 600 650 700 750 800 850 900 950 1000 1050 1100
Time (sec)

Fig. 23

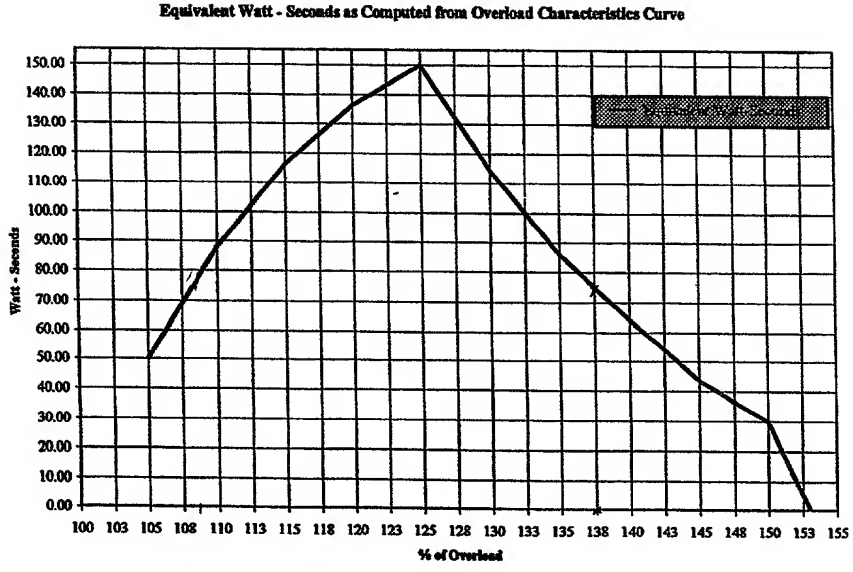

Equivalent Watt - Seconds as Computed from Overload Characteristics Curve
Watt - Seconds
150.00
140.00
130.00
120.00
110.00
100.00
90.00
80.00
70.00
60.00
50.00
40.00
30.00
20.00
10.00
0.00
100 103 105 108 110 113 115 118 120 123 125 128 130 133 135 138 140 143 145 148 150 153 155
% of Overload

Fig. 24

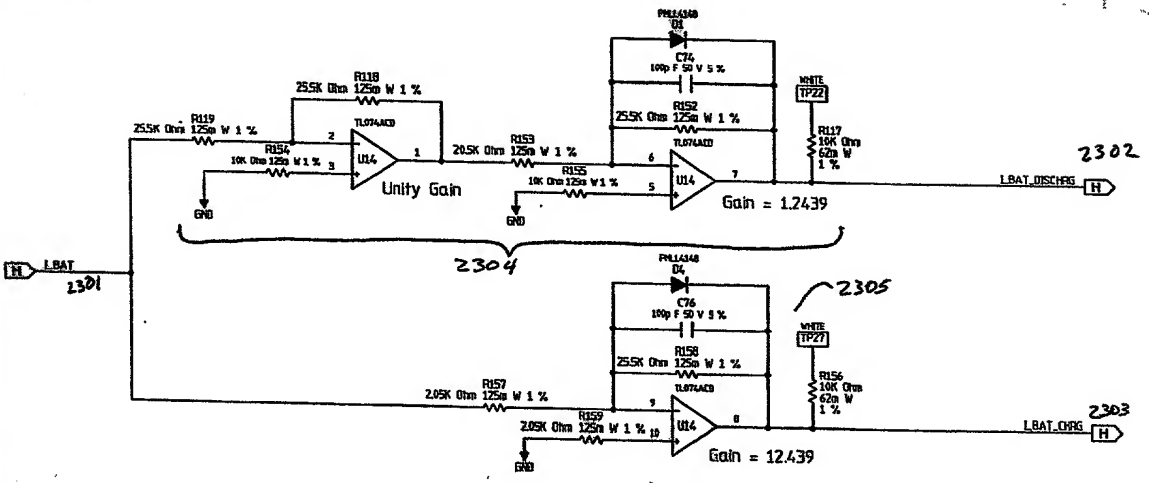

I_BAT
2301
25.5K Ohm 125m W 1 %
R119
R118
25.5K Ohm 125m W 1 %
R154
10K Ohm 125m W 1 %
TL074ACD
U14
Unity Gain
GND
20.5K Ohm 125m W 1 %
R153
R155
10K Ohm 125m W 1 %
GND
C74
100p F 50 V 5 %
R152
25.5K Ohm 125m W 1 %
TL074ACD
U14
Gain = 1.2439
WHITE
TP22
R117
10K Ohm
62m W
1 %
2302
I_BAT_DISCHRG
2304
C76
100p F 50 V 5 %
2305
WHITE
TP27
R158
25.5K Ohm 125m W 1 %
R156
10K Ohm
62m W
1 %
R157
2.05K Ohm 125m W 1 %
R159
2.05K Ohm 125m W 1 %
GND
U14
Gain = 12.439
2303
I_BAT_CHRG

Fig. 25

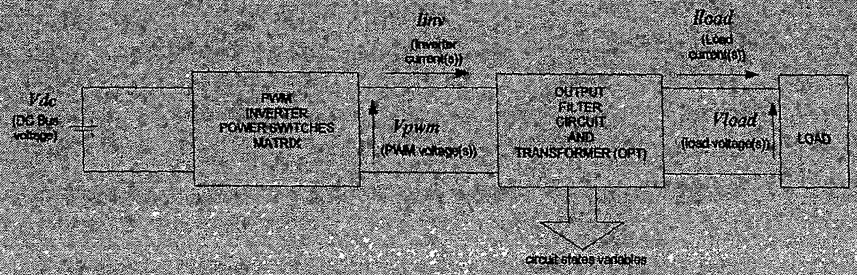

Vdc
(DC Bus voltage)
PWM INVERTER POWER SWITCHES MATRIX
Vpwm
(PWM voltage(s))
Iinv
(Inverter current(s))
OUTPUT FILTER CIRCUIT AND TRANSFORMER (OPT)
Iload
(Load current(s))
Vload
(load voltage(s))
LOAD
circuit states variables

Fig. 26

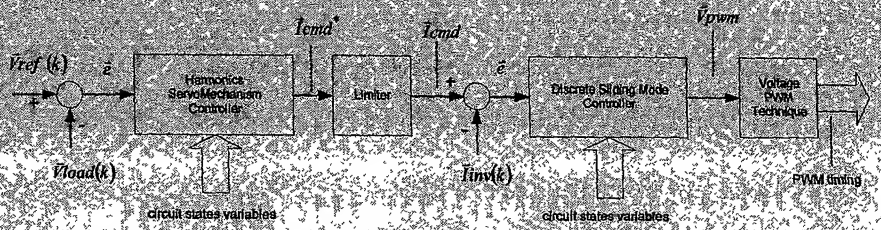

Vref (k)
e
Harmonics ServoMechanism Controller
Icmd*
Limiter
Icmd
e
Discrete Sliding Mode Controller
Vpwm
Voltage PWM Technique
Vload(k)
Iinv(k)
PWM timing
circuit states variables
circuit states variables

Fig. 27

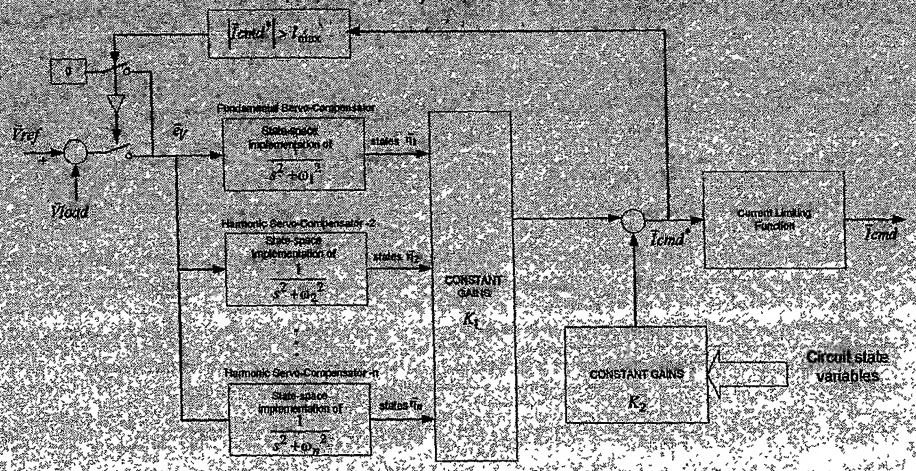

Vref
Vload
Fundamental Servo-Compensator
Harmonic Servo-Compensator -2
Harmonic Servo-Compensator -n
CONSTANT GAINS
K_1
CONSTANT GAINS
K_2
Current Limiting Function
Circuit state variables

Fig. 28

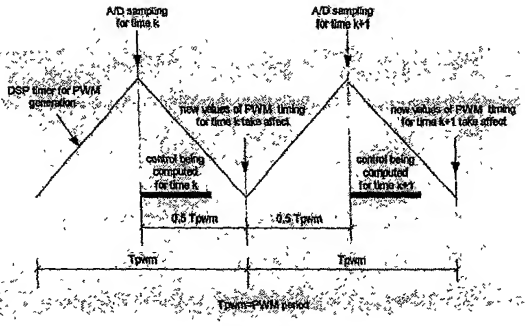

A/D sampling for time k
A/D sampling for time k+1
DSP timer for PWM generation
new values of PWM timing for time k take affect
new values of PWM timing for time k+1 take affect
control being computed for time k
control being computed for time k+1
0.5 Tpwm
0.5 Tpwm
Tpwm
Tpwm
Tpwm=PWM period

Fig. 29

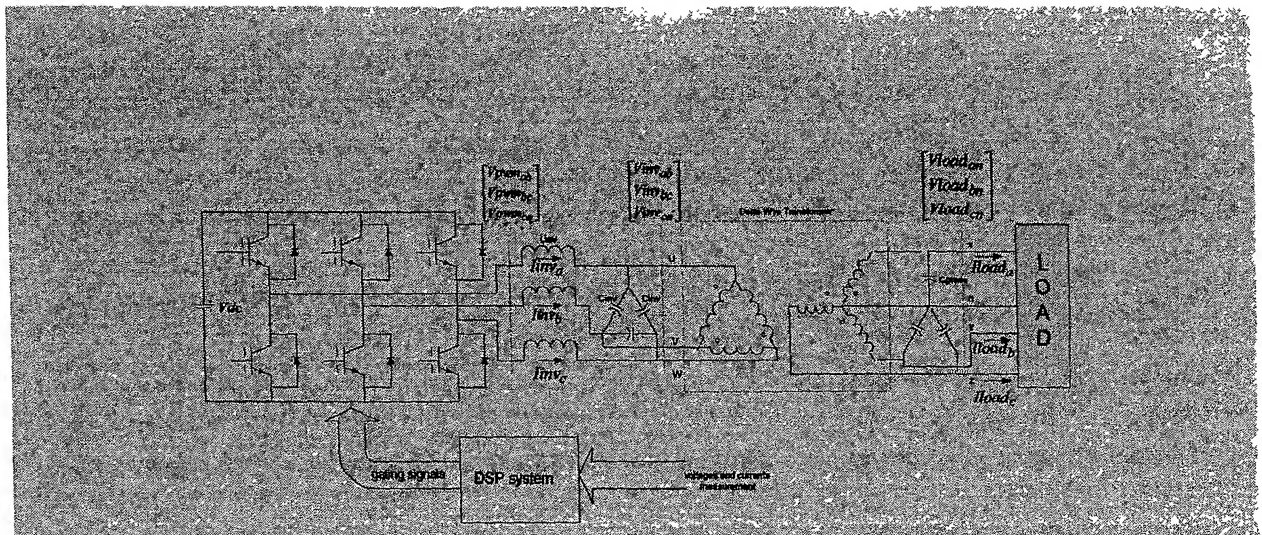

Vpwm_ab
Vpwm_bc
Vpwm_ca
Vinv_ab
Vinv_bc
Vinv_ca
Vload_ab
Vload_bc
Vload_ca
Linv
Iinv_a
Iinv_b
Iinv_c
Vdc
Cinv
Cinv
u
v
w
Iload_a
Iload_b
Iload_c
L
O
A
D
gating signals
DSP system

Fig. 30

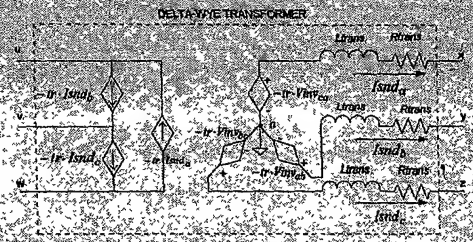

DELTA-WYE TRANSFORMER
Ltrans
Rtrans
Isnd_a
Isnd_b
Isnd_c
tr·Isnd_a
tr·Isnd_b
tr·Isnd_c
tr·Vinv_ab
tr·Vinv_bc
tr·Vinv_ca
u
v
w
x
y
z

Fig. 31

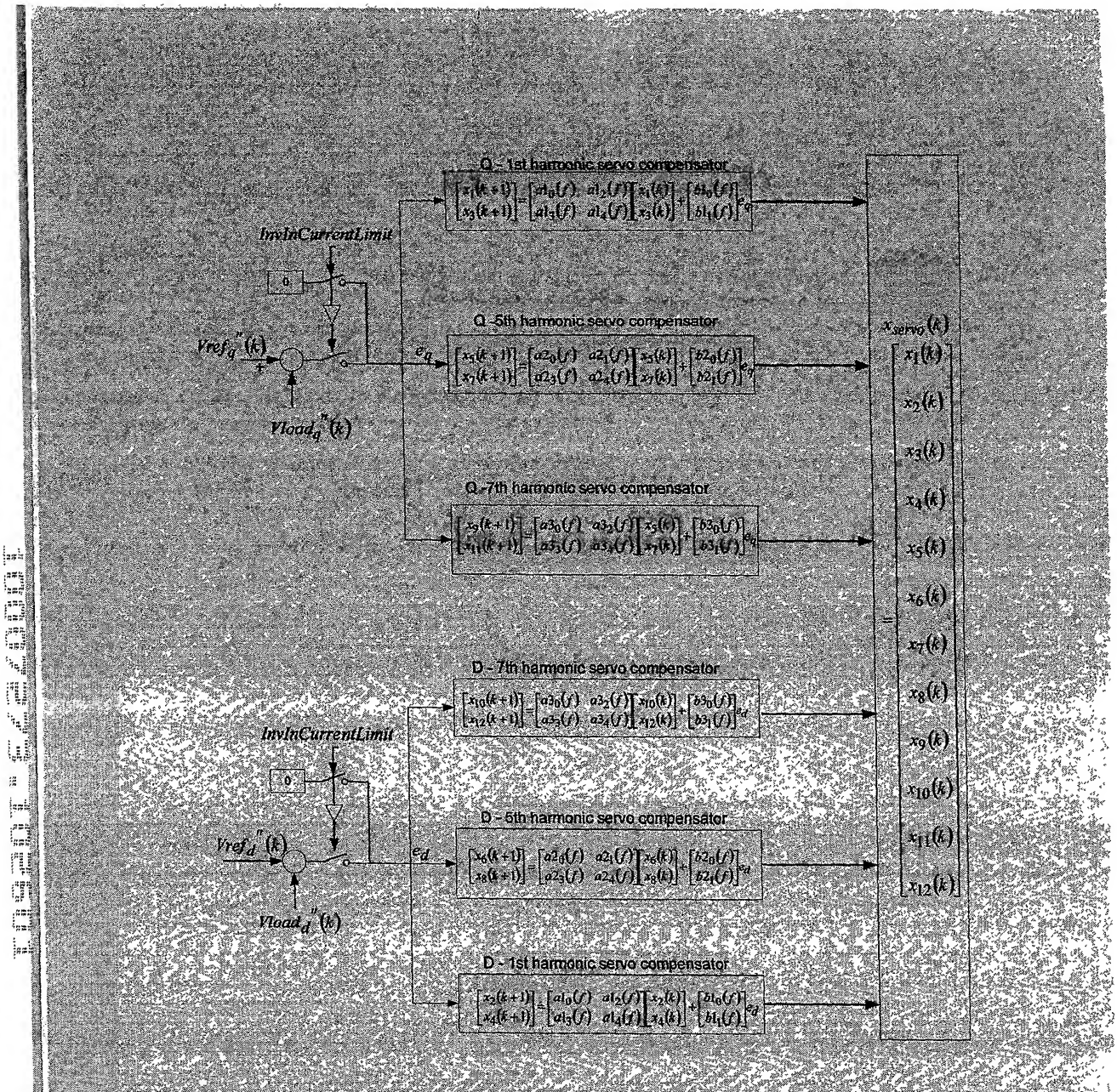


Fig. 32 Discrete time servo compensator

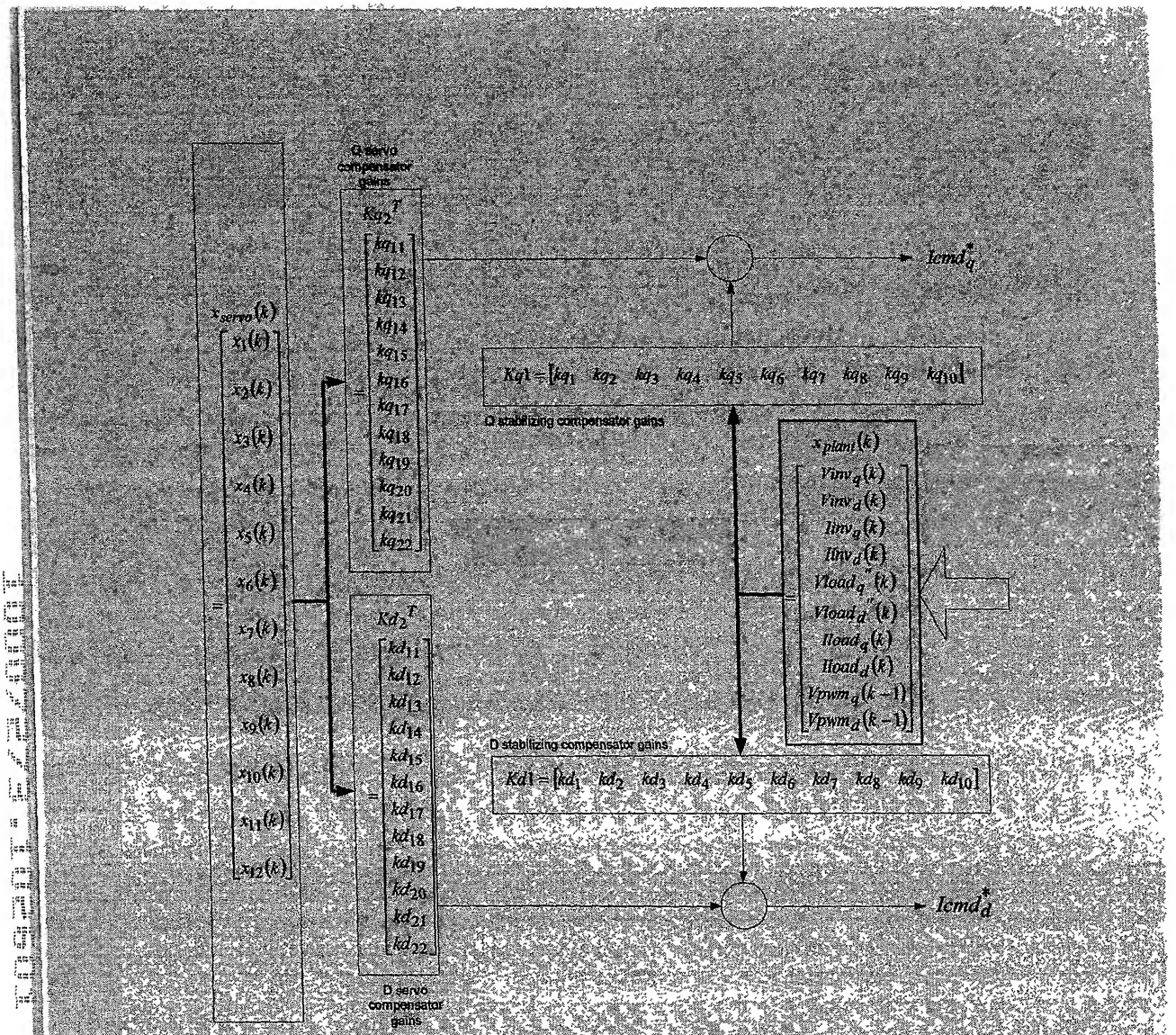


Fig. 33 Discrete time servo compensator (cont.)

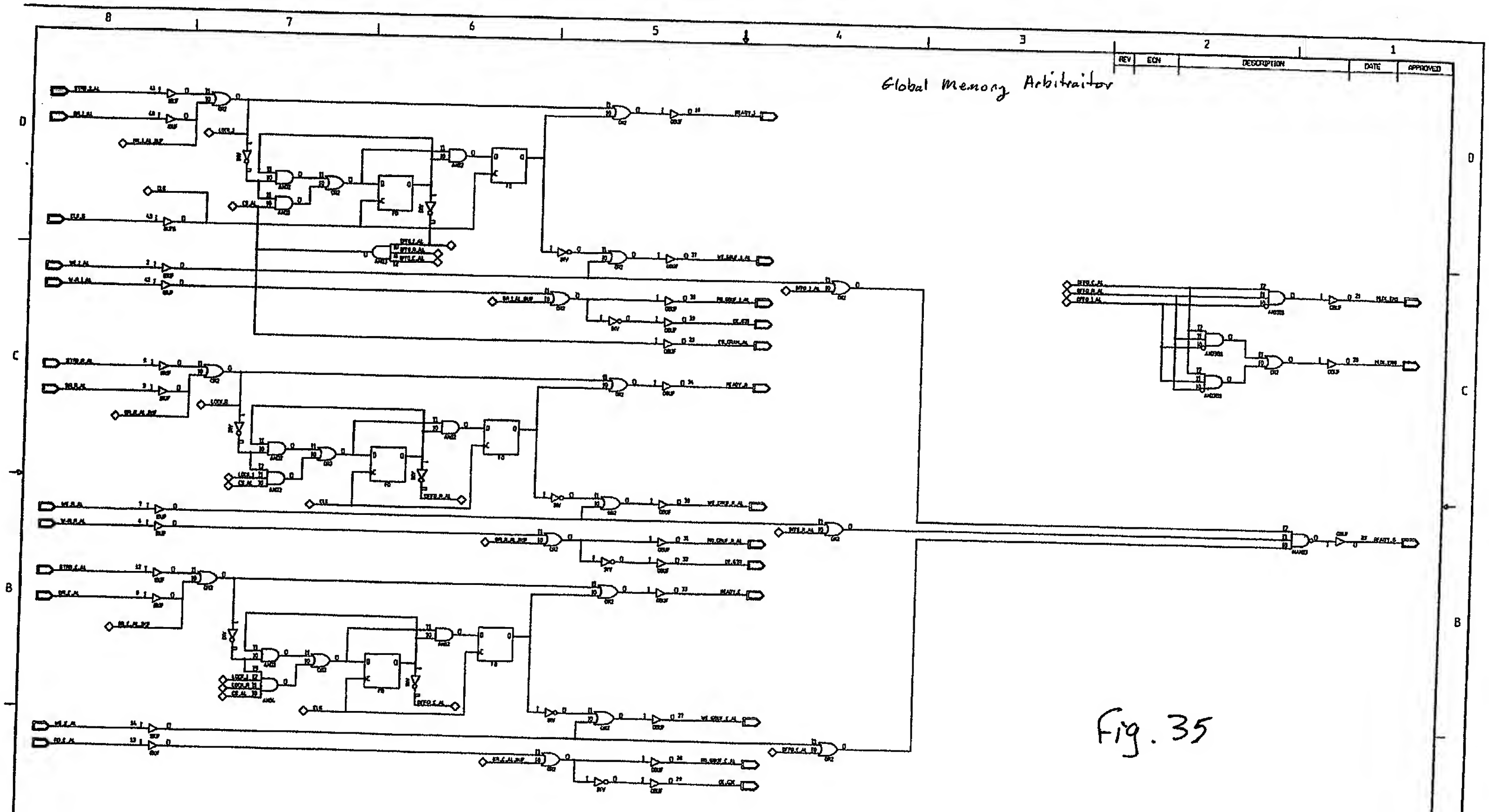


Fig. 35

NOTES:

1. _AL after signal designates the signal as active low

2 The _I, _R, and _C after signals designates Inverter DSP, Rectifier DSP, and Communications DSP, respectively

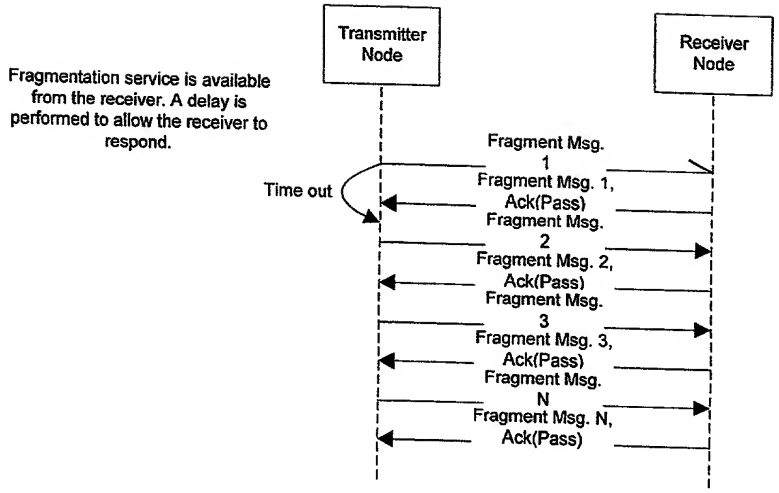

Transmitter Node
Receiver Node
Fragmentation service is available from the receiver. A delay is performed to allow the receiver to respond.
Time out
Fragment Msg. 1
Fragment Msg. 1, Ack(Pass)
Fragment Msg. 2
Fragment Msg. 2, Ack(Pass)
Fragment Msg. 3
Fragment Msg. 3, Ack(Pass)
Fragment Msg. N
Fragment Msg. N, Ack(Pass)

Fig. 36

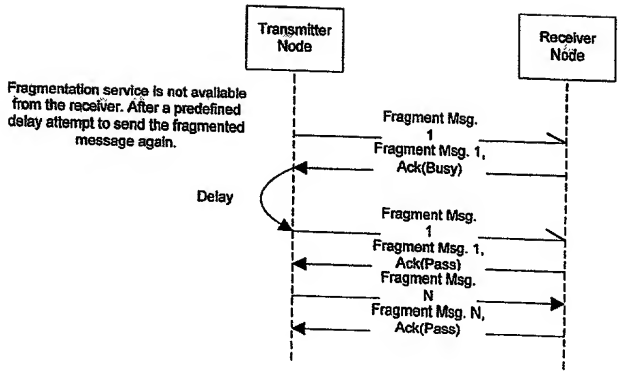

Transmitter Node
Receiver Node
Fragmentation service is not available from the receiver. After a predefined delay attempt to send the fragmented message again.
Fragment Msg. 1
Fragment Msg. 1, Ack(Busy)
Delay
Fragment Msg. 1
Fragment Msg. 1, Ack(Pass)
Fragment Msg. N
Fragment Msg. N, Ack(Pass)

Fig. 37

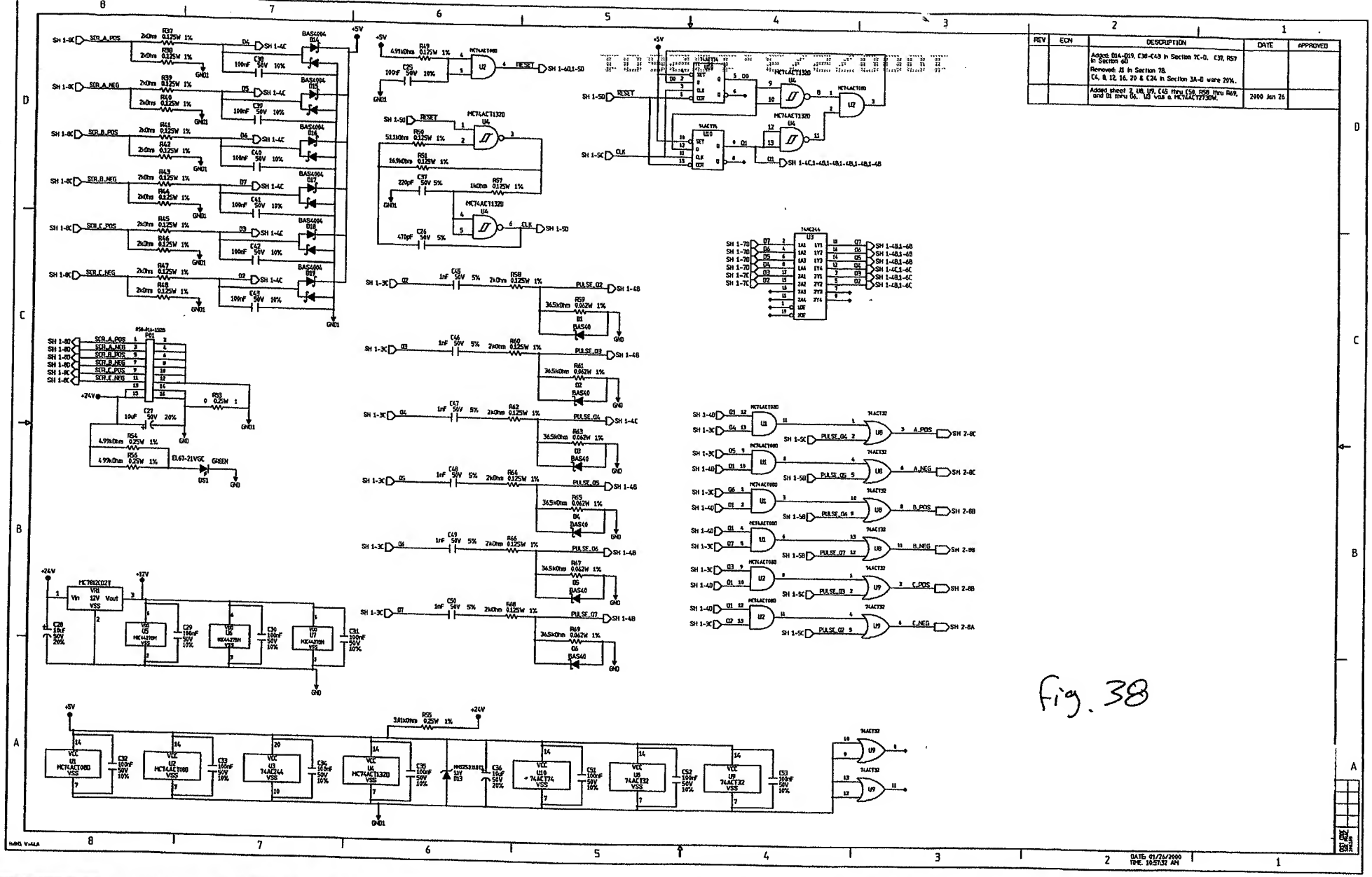

REV
ECN
DESCRIPTION
DATE
APPROVED
Added D14-D19, C38-C43 in Section 7C-D, C37, R57 in Section 6B
Removed J1 in Section 7B.
C4, 8, 12, 16, 20 & C24 in Section 3A-D were 20%.
Added sheet 2. U8, U9, C45 thru C50, R58 thru R69, and J1 thru J6. U3 was a MC74AC273DW.
2000 Jan 26
DATE: 01/26/2000
TIME: 10:57:32 AM

Fig. 38